REMARKS

In response to the Final Office Action mailed October 27, 2003, and the Advisory Action mailed April 22, 2004, the Applicants respectfully request reconsideration.

Applicant notes with appreciation the allowance of claims 19 and 20, and the allowance of claims 12 and 17 if rewritten in independent form.

1. Claims 1 and 6 and 10-14 Patentably Distinguish Over Aiello

Claims 1-6, 10, 11, 13 and 14 stand rejected under 35 U.S.C. §103(a) as purportedly being unpatentable over U.S. Patent No. 5,382,837 (Aiello). Applicants respectfully traverse this rejection.

1.1 Discussion of Aiello

The discussion of Aiello from Applicants' previous response submitted March 17, 2004 is hereby incorporated by reference. Portions thereof relevant to the following discussion have been included below (and elaborated upon) for the Examiner's convenience.

Aiello illustrates several embodiments of a switching circuit (Figs. 1-6). Each embodiment includes a transistor T1 having an emitter connected to a ground potential, a collector connected to a an insulation region (Viso) and a base coupled to a power supply Vcc through a resistor R1. Each embodiment further includes a transistor T2 having an emitter connected to a substrate (Vsub) and a collector connected to Viso. (Figs. 1-6; Col. 3, line 37-col. 6, line 38).

In the embodiments of Figs. 1 and 2, the base of T2 is connected to a reference potential (i.e., ground) through a diode D1. Diode D1 maintains the base of T2 at a constant voltage equal to V_{be}, the base-emitter voltage of T2. (Col. 3, lines 53-58; col. 3, line 67-col. 4, line 1).

Aiello indicates that, when the potential of the substrate is greater than a reference potential (e.g., Vsub > zero), T2 is off and T1 is in saturation mode, thereby coupling the insulation region to the ground voltage. (Col. 3, line 59-col. 4, line 3; col. 4, lines 34-46).

Contrary to the assertions of the Final Office Action (Section 2, page 3, lines 7-11) and the Advisory Action (page 2, third paragraph – page 3), Aiello does not disclose that the insulation region (V_{iso}) is coupled to the substrate (V_{sub}) when a substrate potential is greater than a reference potential and transistor T2 is off. Rather Aiello discloses that **when the substrate**

potential is less than a reference potential (e.g., $V_{sub} < 0$), T2 is in saturation mode. (Col. 4, lines 4-24, 47-54; col. 6, lines 14-17; emphasis added).

1.2 Aiello Does Not Inherently Teach the Claimed Limitation

The Advisory Action states, relying on col. 3, lines 59-68 of Aiello, that:

> "If the substrate potential is 1 volt, e.g. (or any voltage higher than 0), the reference potential can be set at 1.1 volts, e.g. (or any voltage fractionally higher than the substrate potential). This reference potential meets the claimed limitation of a substrate potential being lower than the reference potential, and this substrate potential insures that the first bipolar transaction is off, as taught by Aiello, et al."

Aiello does not explicitly teach or suggest the substrate potential being equal to 1 volt (or any voltage higher than 0) or setting the reference voltage (e.g., ground) equal to 1.1 volts (or any voltage fractionally higher than the substrate potential) if the substrate potential is greater than 0. Thus, the Advisory Action appears to contend that Aiello inherently discloses the claimed limitation--"coupling the isolation region to the substrate... when the substrate potential is lower than the reference potential and the first bipolar transistor is off."--because V_{sub} *might* be 1 volt and the reference potential (ground) *might* be set equal to 1.1 volts. If this is the Advisory Action's position, Applicants respectfully disagree, as the requirements for inherency have not been met.

As set forth in MPEP, Section 2112, "in relying on the theory of inherency, the Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the allegedly inherent characteristics necessarily flows from the teachings of the applied prior art.) Thus relying on inherency requires that the inherent characteristics *necessarily* flow from the teachings of the applied prior art.

Aiello does not inherently teach coupling the insulation region (V_{iso}) to the substrate when the substrate potential (V_{sub}) is lower than the reference potential (ground) and the first bipolar transistor (T2) is off because this limitation does not *necessarily flow* from the teaching of Aiello. Moreover, the Advisory Action fails to provide a basis in fact and/or technical reasoning to support the determination that the above-cited limitation of claim 1 is an inherent characteristic of circuit 1 shown in Aiello. Rather, the Advisory Action provides arbitrary values of a substrate potential and a reference potential that allegedly satisfy the above cited limitation of claim 1, these arbitrary values not taught or suggested by Aiello. Should a next Office Action

take the position that these values necessarily flow from the circuit taught by Aiello, Applicants respectfully request that the Office Action provide the requisite support for this position in accordance with 37 C.F.R. §1.104(d)(2).

1.3 Aiello Would Not Operate As Suggested by the Advisory Action for the Values Proposed in the Advisory Action

Contrary to the assertions of the Advisory Action, if the substrate potential (V_{sub}) of Aiello was equal to 1 volt, and the reference potential was set equal to 1.1 volts or higher, then the transistor T2 would be in saturation, not in the cut-off region (i.e., off). As set forth in Aiello, the base potential of the transistor T2 is fixed at V_{be} by means of the diode D1. Accordingly, if the voltage between the base and the emitter terminals of the transistor T2 is equal to or higher than the value of the voltage across the diode D1, then the transistor T2 is in saturation. Using the following variables for the circuit of Fig. 1: V_{be} as the base-emitter voltage of the transistor T2; V_f as the voltage across the diode D1; V_{ref} as the reference voltage (e.g., ground in Fig. 1); and V_{sub} as the substrate voltage (as indicated in Fig. 1), then by KVL, $V_{be} + V_{sub} = V_f + V_{ref}$. Solving this equation results in: $V_{be} = V_f + .1$, in which case transistor T2 is in saturation -- not in cutoff. Accordingly, Aiello does not teach or suggest, explicitly or inherently, that if the substrate potential is 1.0 volts and the reference potential is set equal to 1.1 volts, then T2 is off (e.g., in the cutoff region).

1.4 Claim 1 Patentably Distinguishes Over Aiello

Claim 1 has been amended as shown above to clarify that the reference potential input provides the reference potential recited in claim 1. This amendment was made solely for clarification, not in response to any rejection or art of record.

Claim 1 is not anticipated by Aiello because Aiello fails to teach or suggest an integrated circuit including, *inter alia*, a first bipolar transistor with an emitter connected to said isolation region and a collector connected to a reference potential input of the integrated circuit, the reference potential input providing a reference potential, and a second bipolar transistor with an emitter connected to the substrate and a base coupled to the isolation region for **coupling the isolation region to the substrate** through a high-impedance **when the substrate potential is lower than the reference potential and the first bipolar transistor is off**, as recited in claim 1.

Rather, as discussed above, Aiello teaches that, when a substrate potential is lower than the reference potential, the first bipolar transistor (T2) is not off, but is operating *in saturation mode*.

In view of the foregoing, claim 1 distinguishes over Aiello. Accordingly, Applicants respectfully request that the rejection of claim 1 under 35 U.S.C. §103(a) as being unpatentable over Aiello be withdrawn.

Claims 2-6 and 10-14 each depend from claim 1 and are patentable for at least the same reasons. Accordingly, Applicants respectfully request that the rejections of claims 2-6, 10, 11, 13 and 14 under Section 103(a) be withdrawn.

2. Claims 7-9 and 15-18 Patentably Distinguish Over Aiello

Claim 7 has been amended as shown above to clarify that the reference potential input provides the reference potential recited in claim 1. This amendment was made solely for clarification, not in response to any rejection or art of record.

Claims 7-9, 15, 16 and 18 stand rejected under 35 U.S.C. § 103(a) as purportedly being unpatentable over Aiello. Applicants respectfully traverse this rejection because Aiello fails to teach or suggest all of the limitation of claim 7, as should be clear from the above discussion relating to claim 1. Specifically, Aiello fails to teach or suggest a semiconductor device, comprising: *inter alia,* a protection structure against polarity inversion of a substrate potential, comprising: a first bipolar transistor having an emitter connected to said isolation region and a collector connected to a reference potential input of the integrated circuit, the reference potential input providing a reference potential; and **means for coupling the isolation region to the substrate** through a high impedance **when the substrate potential is lower than the reference potential *and the first bipolar transistor is off***, as recited in claim 7.

In view of the foregoing, claim 7 distinguishes over Aiello. Accordingly, Applicants respectfully request that the rejection of claim 7 under §103(a) as being unpatentable over Aiello be withdrawn.

Claims 8, 9 and 15-18 each depend directly or indirectly from claim 7 and are patentable over Aiello for at least the same reasons. Accordingly, Applicants respectfully request that the rejections of claims 8, 9, 15, 16 and 18 under §103(a) be withdrawn.

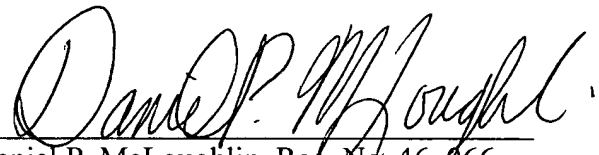
CONCLUSION

In view of the foregoing amendments and remarks, this application should now be in condition for allowance. A notice to this effect is respectfully requested. If the Examiner believes, after this amendment, that the application is not in condition for allowance, the Examiner is requested to call the Applicants' attorney at the telephone number listed below.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicants hereby request any necessary extension of time. If there is a fee occasioned by this response, including an extension fee that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

Antonino Torres, et al., Applicants

By: 

Daniel P. McLoughlin, Reg. No. 46,066
Wolf, Greenfield & Sacks, P.C.
600 Atlantic Avenue
Boston, Massachusetts 02210-2211
Tel. No.: (617) 720-3500
Attorney for Applicants

Docket No.: S1022.80385US00
Date: June 28, 2004

Docket No. S1022.80385US00
Applicant: Antonino Torres, et al.
Serial No. 09/497,916
Filed: February 4, 2000
For: An Integrated Circuit Including Protection Against Polarity Inversion of the Substrate Potential
Annotated Sheet - Fig. 7

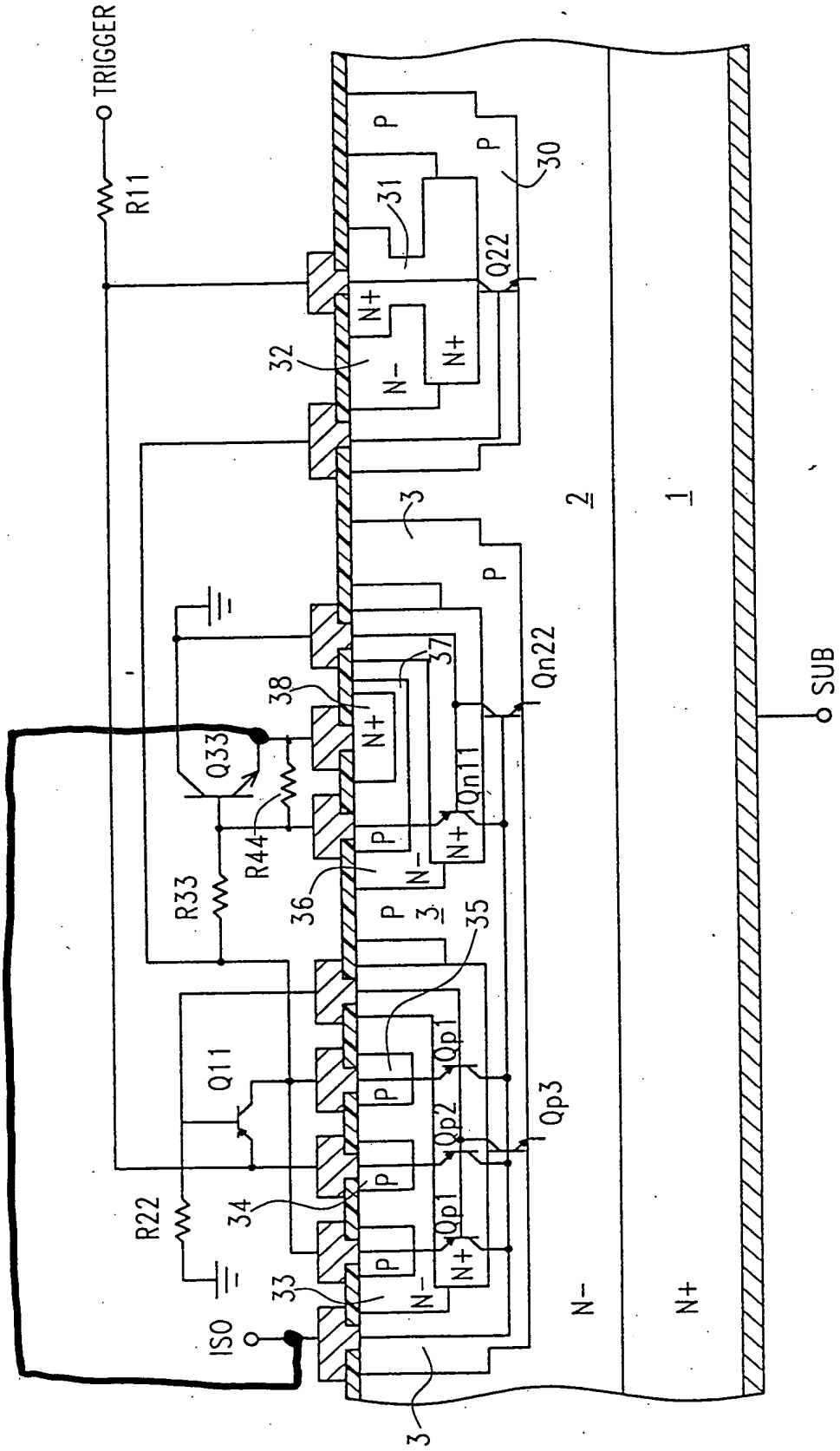


Fig.7